APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,580	11/09/1999	ALEXANDER G. MACINNIS	36101/SAH/B6	8182

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EXAMINER
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ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
		09/437,580	MACINNIS ET AL.
Office Action Summary		Examiner	Art Unit
		Kevin M. Nguyen	2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>21 January 2005</u>.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>26-30,32,33,35-44 and 47-50</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>26-30,32,33,35-44 and 47-50</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/21/05, 1/27/04</u>

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 1-04)   Office Action Summary   Part of Paper No./Mail Date 20050610

DETAILED ACTION

1.   This office action is made in response to applicant's amendment filed on

01/21/2005. Claims 1-25, 31, 34, 45, 46 are cancelled, claims 26, 32, 33, 35, 36, 40, 41,

43, 44 are amended, claims 47-50 are new, and claims 26-30, 32-33, 35-44 and 47-50

are currently pending in the application. An action follows below:

2.   Claims 34 and 45 are cancelled. Thus, the rejection of claims 34 and 45 under 35

U.S.C. 112, second paragraph, is withdrawn.

3.   Applicant's amendment with respect to the claims 26, 32, 33, 35, 36, 40, 41, 43,

44 necessitated the new grounds of rejection presented in this Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 26-30, 32-33, 47, 48, 35-39, 43, 44, 50 are rejected under 35 U.S.C.

103(a) as being unpatentable over Watts et al (newly cited, US 4,412,294) in view of

Fumoto et al (previously cited, US 5,200,738).

5.   As to claim 26, Watts et al teach a method of moving image comprising steps of

showing by Fig. 6, the header data packet is defined by *"source of data*

packet" having region data tables (RDTs) for FORM 2 (1-4), *"destination*

address" having referring to the RDT for region 1 (window) in fig. 6, region 1

character and character attribute data are stored in display memory location 10-

24 (address location of memory, col. 7, lines 33-36), and *"control and timing*

information" having modifying the pointers RA and LA to indicate the memory

location 10-24, see col. 6, lines 60-63), scrolling function including increasing the

smooth scrolled offset one pixel (or scan line per region) per display frame (see

more details in fig. 6, col. 12, lines 35-41) (receiving a header data packet, and

blanking out one or more pixels of the plurality of graphics data).

Fig. 6 expressly showing receiving an address line at 0 (see fig. 6) of an

initial plurality of graphics data (data at 0, see fig. 6) from a memory;

modifying (placing) the pointers RA and LA to indicate the memory

location of the next desired row of characters, i.e., an initial data row at 0, the

displayed window at the new address line "12-19" (see fig. 6, col. 6, lines 60-63)

(even if a starting pixel that is to be displayed is not at the start of address line

"12-19");

deleting lines (blanking out one or more pixels) and scrolling are achieved

by merely modifying the pointers RA and LA to indicate the memory location of

the next desired row of characters. This greatly increases the processing

throughput of CPU 10 because only the affected pointers need to be modified,

without rearranging character and character attribute data in the display memory

(see col. 6, lines 60-66);

inserting lines (inserting new address line) and scrolling are achieved by

merely modifying the pointers RA and LA to indicate the memory location of the

next desired row of characters based on the received header data packet (RDT).

This greatly increases the processing throughput of CPU 10 because only the

affected pointers need to be modified, without rearranging character and

character attribute data in the display memory (see col. 6, lines 60-66);

displaying the new plurality of graphics data "the "after" view of the display

screen show region 3 scrolled up one row of characters, that is, row K is now the

first displayed row of characters and row L is the last displayed row. Also shown

in FIG. 7 is a map of the RA and LA pointers showing the action of the pointers

both before and after the scroll function has been completed" (see col. 7, line 68

to col. 8, lines 6). Smooth scrolling, i.e., the scrolling of a line one pixel or scan

line at a time, may be performed independently in any of the vertical or horizontal

split regions under the control of CRTC 16 (see col. 8, lines 28-32).

Accordingly, Watts et al teach all the subject matter claimed except for the use of

horizontally scrolling instead of horizontally scrolling to the left.

However, horizontally scrolling and horizontally scrolling to the left have

recognized in the art as equivalents as evidenced by Fumoto et al. Fumoto et al it is

noted that the operation for scrolling to the left or right in the horizontal display direction

is basically identical to the vertical operation (see col. 5, lines 36-42).

Therefore, it would have been obvious to one of ordinary skill in the art to replace

horizontally scrolling in Watts et al with horizontally scrolling to the left to achieve the

benefit the method enables scrolling in any arbitrary direction to be easily executed, as

a combination of scrolling in the X and Y directions as taught by Fumoto et al (col. 5,

lines 48-50).

Moreover, where the claimed differences involve substitution of interchangeable equivalents and the reason for the selection of one equivalent for another was not to solve an existent problem such substitution has been judicially determined to have been obvious. See In re Ruff, 118 USPQ 343 (CCPA 1958).

6.   As to claim 27, Fumoto et al teaches display memory contents (fig. 3) to be displayed on the screen including a sequential collection of bits. Each bit in a bit image corresponds to one pixel (dot) on the screen.

7.   As to claim 27, Watts et al teach deleting lines (blanking out one or more pixels) (see col. 6, lines 60-66) comprising the operation deleting lines (pixels) of bits 0-13 are used to select any one of 16K byte addresses in a particular GROM (see more details in col. 5, lines 30-35).

8.   As to claim 28, Watts et al teach the first number (a number of pixel or bit) is not greater than the second number (new data address 12-19, fig. 6).

9.   As to claim 29, Watts et al teach a display memory 96 (a first number) contains 2K 16-bit bytes (col. 5, line 1).

10.   As to claim 30, Watts et al teach GROM (a second number) contains 16K bytes (col. 5, line 33-35).

11.   As to claim 32, Watts et al teach a method of moving image comprising steps of

        Fig. 6 expressly showing receiving an initial address line at 0 (see fig. 6) of an initial plurality of graphics data (data at 0, see fig. 6) from a memory;

        Fig. 6 expressly showing receiving a new address line at 12th (see fig. 6) of a new plurality of graphics data (data at 12th, see fig. 6) from a memory;

modifying the pointers RA and LA to indicate the memory location of the next desired row of characters, i.e., an initial data row at 0, the displayed window at the new address line "12-19" (see fig. 6, col. 6, lines 60-63) (even if a starting pixel that is to be displayed is at the new address line "12-19");

deleting lines (blanking out one or more pixels) and scrolling are achieved by merely modifying the pointers RA and LA to indicate the memory location of the next desired row of characters. This greatly increases the processing throughput of CPU 10 because only the affected pointers need to be modified, without rearranging character and character attribute data in the display memory (see col. 6, lines 60-66);

inserting lines (inserting new address line) and scrolling are achieved by merely modifying the pointers RA and LA to indicate the memory location of the next desired row of characters. This greatly increases the processing throughput of CPU 10 because only the affected pointers need to be modified, without rearranging character and character attribute data in the display memory (see col. 6, lines 60-66);

The "after" view of the display screen show region 3 scrolled up one row of characters, that is, row K is now the first displayed row of characters and row L is the last displayed row. Also shown in FIG. 7 is a map of the RA and LA pointers showing the action of the pointers both before and after the scroll function has been completed (*displaying the new plurality of graphics data*, col. 7, line 68 to col. 8, lines 6). Smooth scrolling, i.e., the scrolling of a line one pixel or

scan line at a time, may be performed independently in any of the vertical or

horizontal split regions under the control of CRTC 16 (see col. 8, lines 28-32).

Accordingly, Watts et al teach all the subject matter claimed except for the use of

horizontally scrolling instead of horizontally scrolling to the right.

However, horizontally scrolling and horizontally scrolling to the right have

recognized in the art as equivalents as evidenced by Fumoto et al. Fumoto et al it is

noted that the operation for scrolling to the left or right in the horizontal display direction

is basically identical to the vertical operation (see col. 5, lines 36-42).

Therefore, it would have been obvious to one of ordinary skill in the art to replace

horizontally scrolling in Watts et al with horizontally scrolling to the right to achieve the

benefit the method enables scrolling in any arbitrary direction to be easily executed, as

a combination of scrolling in the X and Y directions as taught by Fumoto et al (col. 5,

lines 48-50).

Moreover, where the claimed differences involve substitution of interchangeable

equivalents and the reason for the selection of one equivalent for another was not to

solve an existent problem such substitution has been judicially determined to have been

obvious. See In re Ruff, 118 USPQ 343 (CCPA 1958).

12.   As to claim 33, Watts et al teach Fig. 6 expressly showing receiving a new

address line at a start point at 12th and an end point at 19th (see fig. 6) of a new plurality

of graphics data (data at 12th, see fig. 6) from a memory, and one or more pixels at

address 20th to 24th (see fig. 6) are not displayed (the memory locations 12-19 (fig. 6)

comprising the "window" of region1 that is currently displayed (fig. 6, col. 7, lines 40-41).

13.   As to claim 47, Watts et al teach fig. 7 expressly showing line J represents the

first row of characters in region 3 while line K represents the last row of characters. The

"after" view of the display screen show region 3 scrolled up one row of characters, that

is, row K is now the first displayed row of characters and row L is the last displayed row

(col. 7, line 66 to col. 8, lines 3), as modify by Fumoto et al, the operation for scrolling to

the left or right in the horizontal display direction is basically identical to the vertical

operation (see col. 5, lines 36-42).

14.   As to claim 48, Watts et al teach fig. 7 expressly showing line J represents the

first row of characters in region 3 while line K represents the last row of characters. The

"after" view of the display screen show region 3 scrolled up one row of characters, that

is, row K is now the first displayed row of characters and row L is the last displayed row

(col. 7, line 66 to col. 8, lines 3). Thus, the display line K having bits are equal to the

display line L having bits.

15.   As to claim 35, Watts et al teach deleting lines (blanking out one or more pixels)

(see col. 6, lines 60-66) comprising the operation deleting lines (pixels) of bits 0-13 are

used to select any one of 16K byte addresses in a particular GROM (see more details in

col. 5, lines 30-35).

16.   As to claim 36, Watts et al teach the first number (a number of pixel or bit) is not

greater than the second number (new data address 12-19, fig. 6).

17.   As to claim 37, Watts et al teach a display memory 96 (a first number) contains

2K 16-bit bytes (col. 5, line 1).

18.   As to claim 38, Watts et al teach GROM (a second number) contains 16K bytes

(col. 5, line 33-35).

19.   As to claim 39, Watts et al teach the header data packet, as stated *supra* with

respect to claim 26, that scrolls by increasing the smooth scrolled offset one pixel (or

scan line per region) per display frame (see more details in fig. 6, col. 12, lines 35-41)

(receiving a header data packet, and blanking out one or more pixels of the plurality of

graphics data).

20.   As to claim 43, Watts et al teach a graphics display system comprising:

        Fig. 6 expressly showing an initial address line at 0 (see fig. 6) of an initial

plurality of graphics data (data at 0, see fig. 6) from a memory;

        Fig. 6 expressly showing a new address line at 12th (see fig. 6) of a new

plurality of graphics data (data at 12th, see fig. 6) from a memory;

        Dashed line 110 in fig. 1a denotes the expanded portions of the operating

and program storage memory, program instruction are down loaded from the

GROM (a display engine) to the DRAM operating system memory as needed for

execution by CPU 10 (col. 5, lines 12-19);

        Memory locations 0000-1FFF are assigned to system ROM 27 (a direct

access memory module), which contains 2K bytes (expandable to 8K) of

program instructions to control the system initialization and diagnostics on power

up, as well as instructions for loading DRAM 48a from the program storage

memory resident in the GROMs (metal gate read only memories). CPU 10 uses

DRAM 48a for execution of instructions to control the terminal (col. 4, lines 30-37);

The modified pointers RA and LA indicate the memory location of the next desired row of characters, i.e., an initial data row at 0, the displayed window at the new address line "12-19" (see fig. 6, col. 6, lines 60-63) (even if a starting pixel that is to be displayed is at the new address line "12-19");

GROM deletes lines (blanks out one or more pixels) and scrolls are achieved by merely modifying the pointers RA and LA to indicate the memory location of the next desired row of characters. This greatly increases the processing throughput of CPU 10 because only the affected pointers need to be modified, without rearranging character and character attribute data in the display memory (see col. 6, lines 60-66).

Accordingly, Watts et al teach all the subject matter claimed except for the use of horizontally scrolling instead of horizontally scrolling to the right.

However, horizontally scrolling and horizontally scrolling to the right have recognized in the art as equivalents as evidenced by Fumoto et al. Fumoto et al it is noted that the operation for scrolling to the left or right in the horizontal display direction is basically identical to the vertical operation (see col. 5, lines 36-42).

Therefore, it would have been obvious to one of ordinary skill in the art to replace horizontally scrolling in Watts et al with horizontally scrolling to the right to achieve the benefit the method enables scrolling in any arbitrary direction to be easily executed, as

a combination of scrolling in the X and Y directions as taught by Fumoto et al (col. 5,

lines 48-50).

Moreover, where the claimed differences involve substitution of interchangeable

equivalents and the reason for the selection of one equivalent for another was <u>not to</u>

<u>solve an existent problem</u> such substitution has been judicially determined to have been

obvious. See <u>In re Ruff, 118 USPQ 343 (CCPA 1958)</u>.

21.   As to claim 44, Watts et al teach Fig. 6 expressly showing receiving a new

address line at a start point at 12th and an end point at 19th (see fig. 6) of a new plurality

of graphics data (data at 12th, see fig. 6) from a memory, and one or more pixels at

address 20th to 24th (see fig. 6) are not displayed (see the dash line of displayed window

in fig. 6).

22.   As to claim 50, Watts et al teach a header data packet (fig. 6) including the left

edge value (0 value, fig. 6) for indicating a starting location of the graphics window

(region 1, fig. 6), GROM (the display engine) receives the header data packet and

selects and deletes lines (blanks out one or more pixels) by the pointers RA and LA to

indicate the memory location of the next desired row of characters (fig. 6).

Claim Rejections - 35 USC § 102

23.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

24.   Claims 40-42 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by

Watts et al.

25.   As to claim 40, Watts et al teach a graphics display system for moving image

comprising:

Fig. 6 expressly showing the header data packet is defined by *"source of*

data packet" having region data tables (RDTs) for FORM 2 (1-4), *"destination*

address" having referring to the RDT for region 1 (window) in fig. 6, region 1

character and character attribute data are stored in display memory location 10-

24 (address location of memory, col. 7, lines 33-36), and *"control and timing*

information" having modifying the pointers RA and LA to indicate the memory

location 10-24, see col. 6, lines 60-63), scrolling function including increasing the

smooth scrolled offset one pixel (or scan line per region) per display frame (see

more details in fig. 6, col. 12, lines 35-41) (receiving a header data packet, and

blanking out one or more pixels of the plurality of graphics data).

Fig. 6 expressly showing an address line at 0 (see fig. 6) of an initial

plurality of graphics data (data at 0, see fig. 6) from a memory;

Dashed line 110 in fig. 1a denotes the expanded portions of the operating

and program storage memory, program instruction are down loaded from the

GROM (a display engine) to the DRAM operating system memory as needed for

execution by CPU 10 (col. 5, lines 12-19);

Memory locations 0000-1FFF are assigned to system ROM 27 (a direct

access memory module), which contains 2K bytes (expandable to 8K) of

program instructions to control the system initialization and diagnostics on power

up, as well as instructions for loading DRAM 48a from the program storage

memory resident in the GROMs (metal gate read only memories). CPU 10 uses

DRAM 48a for execution of instructions to control the terminal (col. 4, lines 30-

37);

        modified the pointers RA and LA indicate the memory location of the next

desired row of characters, i.e., an initial data row at 0, the displayed window at

the new address line "12-19" (see fig. 6, col. 6, lines 60-63) (even if a starting

pixel that is to be displayed is not at the start of address line "12-19");

        deleting lines (blanking out one or more pixels) and scrolling are achieved

by merely modifying the pointers RA and LA to indicate the memory location of

the next desired row of characters. This greatly increases the processing

throughput of CPU 10 because only the affected pointers need to be modified,

without rearranging character and character attribute data in the display memory

(see col. 6, lines 60-66), the RA and LA pointers associated with each row of

screen information, as described above, will map the location of the next

characters in display memory to be displayed on the screen (col. 7, lines 53-57).

        GROM (the display engine) inserting lines (inserting new address line) and

scrolling are achieved by merely modifying the pointers RA and LA to indicate the

memory location of the next desired row of characters based on the received

header data packet (RDT). This greatly increases the processing throughput of

CPU 10 because only the affected pointers need to be modified, without

rearranging character and character attribute data in the display memory (see

col. 6, lines 60-66).

26.   As to claim 41, Watts et al teach the memory locations 12-19 (fig. 6) comprising

the "window" of region 1 that is currently displayed (fig. 6, col. 7, lines 40-41).

27.   As to claim 42, Watts et al teach inherently the DRAM (the direct memory access

module) does not transfer the blanked pixels to the display engine (GROM).

28.   As to claim 49, Watts et al teach a header data packet (fig. 6) including the left

edge value (0 value, fig. 6) for indicating a starting location of the graphics window

(region 1, fig. 6).

Response to Arguments

29.   Applicant's arguments filed 01/21/2005 have been fully considered but they are

not persuasive. Applicant argues features in the independent claims 26, 32, 33, 35, 36,

40, 41, 43, 44 that are newly recited. Thus, new grounds of rejection have been used.

See the rejections above.

Conclusion

30.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

31.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-

7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone

number for the organization where this application or proceeding is assigned is 703-

872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the Patent Application Information Retrieval system, see

http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the

Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197

(toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KMN
June 10, 2005

XIAO WU
PRIMARY EXAMINER